depositing an anti-reflective coating over the reflective metal material layer;

etching the anti-reflective coating to form a pattern;

trim etching the reflective metal material layer according to the pattern; and

removing portions of the polysilicon layer using the pattern formed from the removed portions of anti-reflective coating.

7. (Once Amended) A method of optimizing optical properties of gate patterning to control gate size in an integrated circuit fabrication process, the method comprising:

providing a reflective metal layer over a gate material layer;

providing a mask layer over the reflective metal layer; and

patterning the gate material layer including selectively etching the mask layer and trim etching the reflective metal layer.

14. (Once Amended) A method of forming a gate in an integrated circuit, the method comprising:

providing a gate material layer;

providing a reflective metal layer over the gate material layer;

providing an anti-reflective coating (ARC) layer over the reflective metal layer;

providing a resist layer over the ARC layer; and

patterning a gate structure in the gate material layer by selectively removing portions of the resist layer, ARC layer, reflective layer, and gate material layer, wherein portions of the reflective layer are removed using trim etching.